Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-25 (Canceled)

26. (New) A frequency synthesizer for producing an output signal based on an input signal and a predetermined control signal, the input signal having an input frequency, the output signal having an output frequency higher than the input frequency, the synthesizer comprising:

a multiphase reference generator having means for generating a plurality of phase signals from the input signal, each phase signal having a frequency substantially equal to the input frequency, and each phase signal being out of phase with the other phase signals by a multiple of a predetermined time interval;

a multiplexer having means for receiving the plurality of phase signals, and having means for selecting one of the plurality of phase signals as a multiplexer output signal; and

a phase selector having means for receiving the predetermined control signal and the multiplexer output signal, and having means for generating a phase selector output signal based on the control signal and the multiplexer output signal;

wherein the phase selector output signal is operatively coupled to the means for selecting one of the plurality of phase signals, and

the multiplexer output signal is the frequency synthesizer output signal.

27. (New) The frequency synthesizer as in claim 26, further comprising a means for selecting a portion of the phase selector output signal operatively coupled to the means for selecting one of the plurality of phase signals of the multiplexer.

28. (New) The frequency synthesizer as in claim 27, wherein the one of the plurality of phase signals is selected as the multiplexer output signal by the phase selector output signal on the occurrence of a rising edge of the multiplexer output.

29. (New) The frequency synthesizer as in claim 27, wherein the one of the plurality of phase signals is selected as the multiplexer output signal by the phase selector output signal on the occurrence of a falling edge of the multiplexer output.

30. (New) The frequency synthesizer as in claim 28 or 29, wherein each successive phase signal selected by the phase selector output signal leads a preceding phase signal by a multiple of the predetermined time interval.

31. (Previously presented) The frequency synthesizer as in claim 27, wherein the phase generator is chosen from the group comprising: a ring oscillator, a Johnson counter circuit, and a delay locked loop circuit.

32. (New) The frequency synthesizer as in claim 26, wherein the predetermined control signal is a predetermined binary word.

33. (New) The frequency synthesizer as in claim 27, wherein the phase selector is a binary digital accumulator having a clock input, an accumulator input, and an accumulator output, wherein the predetermined control signal is operatively coupled to the accumulator input, wherein the multiplexer output signal is operatively coupled to the clock signal, and wherein the accumulator output is operatively coupled to the phase selector output signal.

34. (New) The frequency synthesizer as in claim 28, wherein the binary digital accumulator adds the predetermined binary word to a binary stored value on each

cycle of the multiplexer output signal, and wherein the binary stored value is the accumulator output.

35. (New) The frequency synthesizer as in claim 34, wherein the phase selector output signal is transmitted to the means for selecting one of the plurality of phase signals as a select word.

36. (New) A frequency synthesizer for producing an output signal from an input signal based on a predetermined control signal, the input signal having an input frequency, the output signal having an output frequency higher than the input frequency, the synthesizer comprising:

a multiphase reference generator having means for generating a plurality of phase signals from the input signal, each phase signal having a frequency substantially equal to the input frequency, and each phase signal being out of phase with the other phase signals by a multiple of a predetermined time interval;

a multiplexer having means for receiving the plurality of phase signals, having means for selecting at least two of the plurality of phase signals, and having means for blending/interpolating the at least two of the plurality of phase signals into a multiplexer output signal; and

a phase selector having means for receiving the predetermined control signal and the multiplexer output signal, and having means for generating a phase selector output signal based on the control signal and the multiplexer output signal;

wherein the phase selector output signal is operatively coupled to the means for selecting one of the plurality of phase signals, and

the frequency synthesizer output signal is the multiplexer output signal.

37. (New) The frequency synthesizer as in claim 36, further comprising a means for selecting a portion of the at least two phase selector output signals operatively coupled to the means for selecting one of the plurality of phase signals of the multiplexer.

38. (New) The frequency synthesizer as in claim 37, wherein each successive multiplexer output signal selected by the phase selector output signal leads a preceding multiplexer output signal by a multiple of the predetermined time interval.

39. (Previously presented) The frequency synthesizer as in claim 38, wherein the phase generator is chosen from the group comprising: a ring oscillator, a Johnson counter circuit; and a delay locked loop circuit.

40. (New) The frequency synthesizer as in claim 39, wherein the predetermined control signal is a predetermined binary word.

41. (New) The frequency synthesizer as in claim 40, wherein the phase selector is a binary digital accumulator having a clock input, an accumulator input and an accumulator output, wherein the predetermined control signal is operatively coupled to the accumulator input, wherein the multiplexer output signal is operatively coupled to the clock signal, and wherein the accumulator output is operatively coupled to the phase selector output signal.

42. (New) The frequency synthesizer as in claim 41, wherein the binary digital accumulator adds a predetermined binary control word to a binary stored value on each cycle of the multiplexer output signal, and wherein the binary stored value is the accumulator output.

43. (New) The frequency synthesizer as in claim 42, wherein the phase selector output signal is transmitted to the means for selecting at least two of the plurality of phase signals as a select word.

44. (New) The frequency synthesizer as in claim 44, wherein the at least two selected phase signals are selected based on a portion of a select word.

45. (New) The frequency synthesizer as in claim 45, wherein the multiplexer output signal includes a variable delay determined by a delay between the selected phase signals and a first portion of the select word.

46. (New) A frequency synthesizer comprising:

a phase generator having means for receiving an input signal having a reference frequency and means for generating a plurality of phase signals having a frequency substantially equal to the reference frequency, each phase signal being out of phase with the input signal by a multiple of a predetermined time interval;

a multiplexer having means for receiving the plurality of phase signals, and having means for selecting one of the plurality of phase signals as a multiplexer output signal;

a binary digital accumulator having a clock input, an accumulator input and an accumulator output, the multiplexer output signal being operatively coupled to the clock input; and

a storage means for storing a predetermined control word, the storage means being operatively connected to accumulator input,

wherein

the predetermined control word is added by the binary digit accumulator to a stored value on every cycle of the multiplexer output

the multiplexer output is selected by the selector output and is based on at least one of the plurality of phase signals and

each successive multiplexer output leads its predecessor by a multiple of the predetermined time interval.

47. (New) A method of synthesizing an output signal from based on an input signal and a predetermined control signal, the input signal having an input frequency, the output signal having an output frequency higher than the input frequency, the method comprising the steps of:

(a) generating a plurality of phase signals from the input signal;

(b) selecting one of the plurality of phase signals as a selected phase signal;

(c) generating the output signal from the selected phase signal;

(d) adding the predetermined control word to a stored value to generate a select signal based on the selected phase signal;

(e) selecting one of the plurality of phase signals as the selected phase signal based on at least a portion of the select signal;

(f) repeating steps (c) to (e) for every cycle of the output signal.

48. (New) The method as claimed in claim 47, wherein each successive output signal leads its predecessor by a multiple of the predetermined time interval.

49. (New) The method as in claim 28 wherein step (b) includes selecting at least two phase signals from the plurality of phase signals based on at least a portion of the select word, and wherein step (c) includes blending the at least two selected phase signals to generate the output signal.

Appl. No. 10/259,889
Amdt. dated December 12, 2003
Reply to Office Action of September 26, 2003

Amendments to the Drawings:

Attachment: Replacement sheets of formal drawings.